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| 10/733,840 | 12/11/2003 | Alex Chughen Chow | AUS920030713US1 | 2185 |

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| EXAMINER | |
|---|---|
| TRUONG, CAMQUY | |

| ART UNIT | PAPER NUMBER |
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| 2195 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/733,840 | CHOW, ALEX CHUGHEN | |
| | Examiner | Art Unit | |
| | CAMQUY TRUONG | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,5,6,9,10,12,13,15,16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,5-6,9-10,12-13,15-16 and 19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *DETAILED ACTION*

1. Claims 1- 2, 5-6, 9-10, 12-13, 15-16, and 19-20 are presented for examination.

Claims 3-4, 7-8, 11, 14, 17-18, 21-22 have been cancelled.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-2, 5-6, 15-16, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundaresan (U.S. Patent 6,289,369 B1) in view of Phelan (U.S. Patent 4,497,979).**

4. As to claim 1, Sundaresan teaches the invention substantially as claimed

including: a method for load balancing in a tightly-coupled multiprocessor computer system comprising the steps of:

dividing a task into a plurality of subtasks (the execution of a computer is divided into multiple threads, col. 1, lines19-23);

placing the plurality of subtasks into a centralized task queue (Fig. 2; threads 22 resident in the central schedule queue 26, col. 5, lines 62-63);

distributing the plurality of subtasks in the centralized task queue to a plurality of library processors (threads 22 can migrate among processor 10, col. 5, lines 62-64; col. 8, lines 24-27);

wherein at least one subtask from the plurality of subtasks in the centralized task queue is distributed tot at least one of the plurality of library processors when the library processor has at least one empty task buffer (if there is no eligible thread in the per-processor local queue, then the thread from the central queue is dispatched for execution, col. 8, lines 58-60); and

wherein distributing a subtask from the plurality of tasks in the centralized task queue to the one of the plurality of library processors comprises the one of the plurality of library processors fetching the subtask from the centralized task queue (processors take threads from this central ready queue and run them to completion, col. 2, lines 11-12 / the thread 22 remains in the schedule queue 26 until it is dispatched for execution by the scheduler 24, col. 7, lines 1-2; col. 8, lines 58-60).

5. Sundaresan does not explicitly teach each library processor comprise exactly two task buffers. However, Phelan teaches each library processor comprise exactly two task buffers (the first and second queue designated Q1 and Q2, respectively, have been defined in memory 300 associated with processor 301, col. 5, lines 37-40).

6. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Sundaresan to incorporate the teaching of each library processor comprise exactly two task buffers as taught by Phelan because this allows to balance the service requests among system when the system is in the overload conditions.

7. As to claim 2, Sundaresan teaches distributing the subtask from the plurality of subtasks in the centralized task queue to the one of the plurality of library processors when the one of the plurality of library processors has one or two empty task buffers (col. 8, lines 58-61).

8. As to claims 5-6, Sundaresan teaches distributing the task from the plurality of subtasks in the centralized task queue to the one of the plurality of library processors by the one of the plurality of library processors fetching it from the centralized task queue when the load of the one of a plurality of library processors is zero or one subtasks (the thread 22 remains in the schedule queue 26 until it is dispatched for execution by the scheduler 24, col. 7, lines 1-2; col. 8, lines 58-60).

9. As to claim 15, it is rejected for the same reason as claim 1.

10. As to claim 16, it is rejected for the same reason as claim 2.

11. As to claims 19-20, it is rejected for the same reason as claims 5-6.

12. **Claims 9-10, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundaresan (U.S. Patent 6,289,369 B1) in view of Phelan (U.S. Patent 4,497,979), and further in view of Willen et al. (U.S. Patent 7,159,221).**

13. As to claim 9, Sundaresan teaches the invention substantially as claimed including: a method for load balancing in a tightly-coupled multiprocessor computer system comprising the steps of:

Dividing a task into a plurality of subtasks (the execution of a computer is divided into multiple threads, col. 1, lines19-23);

placing the plurality of subtasks into a centralized task queue (Fig. 2; threads 22 resident in the central schedule queue 26, col. 5, lines 62-63);

distributing the plurality of subtasks in the centralized task queue to a plurality of library processors (threads 22 can migrate among processor 10, col. 5, lines 62-64; col. 8, lines 24-27);

wherein at least one subtask from the plurality of subtasks in the centralized task queue is distributed tot at least one of the plurality of library processors when the library processor has at least one empty task buffer (if there is no eligible thread in the per-processor local queue, then the thread from the central queue is dispatched for execution, col. 8, lines 58-60); and

wherein distributing a subtask from the plurality of tasks in the centralized task queue to the one of the plurality of library processors comprises the one of the plurality of library processors fetching the subtask from the centralized task queue (the thread 22 remains in the schedule queue 26 until it is dispatched for execution by the scheduler 24, col. 7, lines 1-2; col. 8, lines 58-60).

14. Sundaresan does not explicitly teach each library processor comprise exactly two task buffers. However, Phelan teaches each library processor comprise exactly two task buffers (the first and second queue designated Q1 and Q2, respectively, have been defined in memory 300 associated with processor 301, col. 5, lines 37-40).

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Sundaresan to incorporate the teaching of each library processor comprise exactly two task buffers as taught by Phelan because this allows to balance the system's overload conditions, service may be degraded to the point where delays in getting dial tone are experienced by the customers.

16. Sundaresan and Phelan do not explicitly teach a system kernel. However, Willen teaches a system kernel (Fig. 2; col. 5, lines 54-55).

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching Sundaresan and Phelan to incorporate the teaching of system kernel as taught by Willen because this allows to balance the system load while minimizing the overhead of fetching cached data from remote cache memories (col. 3, lines 12-14).

18. As to claim 10, Sundaresan teaches each of the plurality of library processors is further configured to fetch a subtask from the library task queue when that library processor has at least one empty task buffer (col. 8, lines 58-61).

19. As to claims 12-13, Willen teaches the system kernel is comprised of a single processor and a plurality of processors (Fig. 2; col. 5, lines 49-53).

***Response to the argument***

20. Applicant arguments filed on 12/1/2008 had been considered but they are not persuasive.

In the remarks applicant argued (1) Sundaresan does not explicitly teach each library processor comprise[s] exactly two task buffers. (2) The Examiner claims it would have been obvious to one of ordinary skill in the art "to incorporate the teaching of each

library processor comprise exactly two task buffers as taught by Phelan because this allows to balance the system's overload conditions, service may be degraded to the point where delays in getting dial tone are experienced by the customers." Office Action, Page 4. Applicants respectfully note that nowhere is there any motivation to provide a telephone dial tone in the Sundaresan reference for "AFFINITY, LOCALITY, AND LOAD BALANCING IN SCHEDULING USER PROGRAM-LEVEL THREADS FOR EXECUTION BY A COMPUTER SYSTEM." Applicants respectfully object to the Examiner's stated motivation as insufficient and irrelevant. (3) "Sundaresan does not explicitly teach a task is distributed when the library processor has at least one empty task buffer. (4) Sundaresan does not explicitly teach a task is distributed when the library processor has an empty buffer.

21. Examiner respectfully traverses Applicant's remarks:

As to point (1), Examiner interprets "each processor has exactly two task buffers" as each processor has two buffers. Applicant fails to clearly define the limitation "each processor has exactly two tasks buffers and the buffers contain tasks" wherein each processor's buffer has exactly two tasks. Phelan discloses each processor has Q1 and Q2 (col. 5, lines 37-40). Thus, it meeting the limitation each processor has exactly two tasks buffers. MPEP required that "Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F. 3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claims. E-Pass Techs.,

Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily". In re Prater, 415 f.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

As to point (2), Sundaresan teaches load balancing in scheduling user program level threads (tasks) for execution by a computer system (col. 1, lines 11-12) while Phelan teaches during the overloads ,a service requests (tasks) are put in common queue to be examined and executed (abstract, col. 2, lines 25-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Sundaresan to incorporate the teaching of each library processor comprise exactly two task buffers as taught by Phelan because this allows to balance the service requests among system when the system is in the overload conditions.

As to point (3), Examiner interprets "the library processor has at least one empty task buffer" as the library processor has at least one buffer wherein the buffer has no task in it. Sundaresan discloses the library processor has at least one empty task buffer (if there is no eligible thread in the per-processor local queue (the local queue is empty), then the thread from the central queue is dispatched for execution, col. 8, lines 58-60).

As to claim 4, Sundaresan teaches a task is distributed when the library processor has an empty buffer (processors take threads from this central ready queue and run them to completion, col. 2, lines 11-12 / the thread 22 remains in the schedule queue 26 until it is dispatched for execution by the scheduler 24, col. 7, lines 1-2; col. 8, lines 58-60).

22. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAMQUY TRUONG whose telephone number is (571)272-3773. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Camquy Truong

February 28, 2009